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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,930	09/19/2003	Warren M. Farnworth	2269-5529US (02-0766.00/U	6453

24247 7590 08/06/2008

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
08/06/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	10/666,930	FARNWORTH ET AL.	
	Examiner	Art Unit	
	STANETTA D. ISAAC	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 25-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 25-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/22/07,3/6/07,9/07/07,10/15/07,1/2/08 & 4/23/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Appeal Brief filed on 3/07/08. Currently, claims 1-14 and 25-39 are pending.

Examiner's Remarks

After further consideration of the Appeal Brief filed on 3/07/08, the Examiner has re-open prosecution on the merits. Please, see rejections below.

Information Disclosure Statement

The information disclosure statements (IDS) were submitted on 1/22/07, 3/06/07, 9/07/07, 10/15/07, 1/02/08, and 4/23/08. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 11-14, and 29-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Tandy et al (US Patent Application Publication, US 2003/0003688 A1, hereinafter referred to as "Tandy").

Tandy discloses the semiconductor method as claimed. See figures 1A-6, and corresponding text, where Tandy teaches, pertaining to claim 1, a method for supporting wafers for singulation and pick-and-place, comprising: providing a semiconductor wafer **10** (figure 1A; [0028]); mounting an adhesive-coated tape **1/2** to a surface of the semiconductor wafer (figure 4A; [0034] and [0039], specific adhesive material); gripping the semiconductor wafer along at least a portion of the periphery thereof (figure 4A; [0034]), ***Note***: the Examiner takes the position that, the marking tape, as taught by Tandy, is bonded to the backside of the semiconductor wafer by an adhesive material, thus, gripping the semiconductor wafer including the periphery at the outer edge portions of the wafer is anticipated); singulating individual components **20** from the semiconductor wafer, leaving a ring of material (portions between the backside surface **24** and outer edge of the wafer **10**) comprising at least in part a material of the semiconductor wafer along the periphery thereof (figure 1A; [0028]); and removing at least some of the individual components **20** from the adhesive-coated tape (figures 4A and 4B; [0034-0035]).

Tandy teaches, pertaining to claim 2, wherein gripping the semiconductor wafer along at least a portion of the periphery thereof further includes gripping the semiconductor wafer by the ring of material during the removing of the at least some individual components (figures 4A and 4B;[0034-0035]).

Tandy teaches, pertaining to claim 3, further including forming the ring of material only from the material of the semiconductor wafer (figure 1A; [0028]).

Tandy teaches, pertaining to claim 4, further including forming at least a portion of the ring of material from a polymer material **2** disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer

(figure 4A; [0039], ***Note***: the Examiner takes the position that the adhesive layer, as taught by Tandy, includes a polymer material attached directly to the backside of the semiconductor wafer including the periphery of the wafer).

Tandy teaches, pertaining to claim 5, further including forming the ring of material in part from the material of the semiconductor wafer and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer (figure 4A;[0039]).

Tandy teaches, pertaining to claim 6, further comprising the ring of material from the polymer material by one of spin-coating, stereolithography or molding ([0039]).

Tandy teaches, pertaining to claim 7, further comprising backgrinding the semiconductor wafer prior to singulating (figure 1B; [0028]).

Tandy teaches, pertaining to claim 11, wherein mounting the adhesive-coated tape comprises mounting a tape bearing a UV-sensitive adhesive thereon ([0033]).

Tandy teaches, pertaining to claim 12, further comprising exposing the UV-sensitive adhesive prior to removing the at least some individual components, while leaving a portion on the adhesive-coated tape extending over the ring of material unexposed ([0035-0036]).

Tandy teaches, pertaining to claim 13, wherein the semiconductor wafer is singulated using one of laser cutting, water cutting and sawing (figure 1A; [0028]).

Tandy teaches, pertaining 14, further comprising discarding the ring of material, any remaining individual components and the adhesive-coated tape after removing the at least some individual components ([0051], ***Note***: the Examiner takes the position since Tandy teaches, the use of conventional semiconductor die testing procedures used to determine good dies,

discarding of materials including adhesive coated tapes and any remaining individual components are anticipated).

Tandy teaches, pertaining to claim 29, a method of processing a semiconductor wafer, comprising: gripping a semiconductor wafer along at least a portion of a periphery thereof (figure 4A; [0034]), ***Note***: the Examiner takes the position that, the marking tape, as taught by Tandy, is bonded to the backside of the semiconductor wafer by an adhesive material, thus, gripping the semiconductor wafer including the periphery at the outer edge portions of the wafer is anticipated); and singulating individual components from the semiconductor wafer while leaving an uncut peripheral ring of material comprising at least in part a material of the semiconductor wafer thereabout (figure 1A; [0028], portions between the backside surface **24** and outer edge of the wafer **10**).

Tandy teaches, pertaining to claim 30, further including removing at least some singulated individual components therefrom (figures 4A and 4B; [0034-0035]).

Tandy teaches, pertaining to claim 31, wherein gripping a semiconductor wafer along at least a portion of a periphery thereof further includes gripping the uncut peripheral ring of material while removing the at least some singulated individual components therefrom (figures 4A and 4B; [0034-0035]).

Tandy teaches, pertaining to claim 32, further comprising defining the uncut peripheral ring of material from semiconductor material (figure 1A; [0028]).

Tandy teaches, pertaining to claim 33, further comprising defining the uncut peripheral ring of material at least in part from polymer disposed about and contiguous with the semiconductor wafer (figure 4A; [0039], ***Note***: the Examiner takes the position that the adhesive

layer, as taught by Tandy, includes a polymer material attached directly to the backside of the semiconductor wafer including the periphery of the wafer).

Tandy teaches, pertaining to claim 34, further comprising defining the uncut peripheral ring of material in part from semiconductor material and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer (figure 4A;[0039]).

3. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Kurosawa (US 7,140,951, hereinafter referred to as "Kurosawa").

Kurosawa teaches, pertaining to claim 25, a method for processing a semiconductor wafer, comprising: mounting an adhesive-coated tape **22** to a surface of a semiconductor wafer **21** (figure 20A; col. 9, lines 43-46); and singulating individual components from the semiconductor wafer and removing at least some singualated individual components without using a film frame while the adhesive-coated tape is mounted to the surface thereof (figures 20A, 23-25; col. 9, lines 50-61; col. 10, 18-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tandy et al (US Patent Application Publication, US 2003/0003688 A1, hereinafter referred to as "Tandy") as applied to claim 1 above, and further in view of Kurosawa (US Patent 7,140,951, hereinafter referred to as "Kurosawa").

5. Tandy discloses the semiconductor method substantially as claimed. See rejection above

6. However, Tandy fails to show, pertaining to claim 8, further comprising mounting the adhesive-coated tape to an active surface of the semiconductor wafer and singulating the semiconductor wafer from a backside thereof after backgrinding. In addition, Tandy fails to show, pertaining to claims 9 and 10, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof.

7. Kurosawa teaches, pertaining to claims 8-10, forming an adhesive layer on the rear surface of the semiconductor wafer and singulating the semiconductor wafer to forming individual discrete semiconductor elements (figure 20A; col. 9, lines 45-51).

8. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the following steps of: further comprising mounting the adhesive-coated tape to an active surface of

the semiconductor wafer and singulating the semiconductor wafer from a backside thereof after backgrinding; further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof, in the method of Tandy, pertaining to claim 8-10, according to the teachings of Kurosawa, with the motivation that by including an adhesive-coat tape on either the active surface or backside of the semiconductor wafer and then singulating the semiconductor wafer an elimination of die chipping cracking and/or scratching is obtained, thus improving the quality of the semiconductor die and increasing the manufacturing yield.

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurosawa (US Patent 7,140,951, hereinafter referred to as "Kurosawa") as applied to claim 25 above, and further in view of Oka (US Patent 6,551,906, hereinafter referred to as "Oka").

Kurosawa discloses the semiconductor method substantially as claimed. See above rejection.

However, Kurosawa fails to show, pertaining to claim 26, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. In addition, Kurosawa fails to show, pertaining to claim 27 further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck. Also, Kurosawa fails to show, pertaining to claim 28, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps: wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers; further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom, in the method of Kurosawa, pertaining to claims 26-28, according to the teachings of Oka, with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tandy et al (US Patent Application Publication, US 2003/0003688 A1, hereinafter referred to as "Tandy") as applied to claim 29 above, and further in view of Oka (US Patent 6,551,906, hereinafter referred to as "Oka").

9. Tandy discloses the semiconductor method substantially as claimed. See above rejection.

However, Tandy fails to show, pertaining to claim 35, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. In addition, Tandy fails to show, pertaining to claim 36 further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck. Also, Tandy fails to show, pertaining to claim 37, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom. Tandy fails to show, pertaining to claim 38, a method of using 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers. Finally, Tandy fails to show, pertaining to claim 39, further including processing the 300 mm Semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps of: wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers; further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at

least some singulated individual components therefrom; a method of using 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers; further including processing the 300 mm Semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers, in the method of Tandy, pertaining to claims 35-39, according to the teachings of Oka, with the motivation that with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STANETTA D. ISAAC whose telephone number is (571)272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
July 29, 2008

/Charles D. Garber/
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